REMARKS

Claims 1-15 are currently pending in the case. No claims were amended in this response.

The applicant has studied the Office Action dated December 16, 2003 and has made the changes believed appropriate to place the application in condition for allowance. Reconsideration and reexamination are respectfully requested.

Applicant acknowledges with thanks the indication of allowance of Claims 2-11 and 15.

The title has been amended to recite "Novel BiCMOS Inverter" as kindly suggested by the Examiner.

Applicant has amended paragraph [0001] to delete the reference to Applicant's priority application. Applicant still maintains Applicant's claim of priority to this Japanese application.

Applicant thanks the Examiner for the telephone interview conducted with attorney William Konrad for this case on Feb. 2, 2004, in which the rejection of the claims was discussed. Mr. Konrad discussed certain aspects of the rejection that are set forth in the discussion below. Agreement was not reached regarding the claims. The Examiner agreed to further consider the remarks set forth in this response.

No claims have been amended in this response. However, as set forth above, the specification has been amended as requested by the Examiner. It is respectfully submitted that these amendments will not require a new search or raise new issues for consideration by the Examiner. It is submitted that these amendments to the specification place the application in better form for appeal. These amendments to the specification were not presented earlier because they were deemed appropriate to advance prosecution after receipt of the latest Office Action. The Examiner is therefore respectfully requested to enter and consider these amendments to the specification after the final rejection.

Claims 1, 12, 13 and 14 have been rejected under 35 U.S.C. 103(a) as being unpatentable over WOLF "Silicon Processing for the VLSI Era" in view of Manning (6,137,146) and Schwank et al. (6,268,630). This rejection is respectfully traversed.

Claim 1 is directed to a semiconductor device comprising, *inter alia*, a field effect transistor and a bipolar transistor wherein "the first body region of the second conduction type is

in contact with and thereby electrically connected to the first base region of the second conduction type ..." The Examiner has conceded that, in addition to other deficiencies, Wolf "does not disclose ... placing the first body region of the second conduction type in contact with and electrically connected to the first base region of the second conduction type ... ." In an attempt to overcome this deficiency of the Wolf reference, the Examiner has taken the position that it would be "obvious ... to place the first body region of the second conduction type of Wolf's semiconducting device in contact with and electrically connected to the first base region of the second conduction type such as taught by Manning, in order to save space on the surface of the semiconducting device to thus increase the density of the logic circuitry." The applicant strongly disagrees.

It is respectfully submitted that the references have been improperly combined and that the rejection of the claims based upon this improper combination should be withdrawn. The Examiner has cited no teaching, suggestion or recognition in the Manning reference of "sav[ing] space on the surface of the semiconducting device."

On the contrary, the Examiner appears to be impermissibly using hindsight, that is, using the present applicants' disclosure to provide a motivation for combining the references, which motivation is wholly lacking from the Examiner's citations to the references. More specifically, the present applicant explicitly teaches:

> *Accordingly, by the manufacturing method in accordance with the present embodiment, the first p-type base region 220 can be electrically connected to the first p-type body region 50a without forming a contact layer for leading out the p-type base region 220.*
> Present specification, page 29, lines 13-16.

The Examiner has cited no teaching or suggestion in the Manning or Wolf references that a base region can be electrically connected to a body region to save surface space by not forming a contact layer for leading out the base region. Instead, the Examiner appears to be impermissibly engaged in using hindsight.

Furthermore, it is respectfully submitted that the Examiner is factually mistaken. Fig. 9 of the Manning reference relied upon by the Examiner, clearly shows a base contact and contact region 46 which are labeled "B" in Fig. 8. Thus, in addition to lacking any teaching, suggestion

or recognition in the Manning reference of "sav[ing] space on the surface of the semiconducting device" by having a base region electrically connected to a body region, the Manning reference clearly teaches providing a space *consuming* contact and contact region for the base region 26c, even though the base region 26c and body region of the Manning reference appear to be in contact.

Lacking any citation to any reference for support, the Examiner has taken the position that "one of ordinary skill in the art would realize the advantages, in terms of cost and functionality, involved in reducing the size of an individual device and thus allowing more devices per chip." December 16, 2003 Office Action, page 14. Whether or not this statement is true as a general matter, it is clearly inapplicable to the present application where the Examiner has cited no teaching or suggestion in any of the references that having a base region electrically connected to a body region can reduce the size of a device. On the contrary, it has been demonstrated above, that the Manning reference clearly teaches the exact opposite. That is the Manning reference shows a space *consuming* base contact and contact region 46 notwithstanding that the base region 26c and body region of the Manning reference appear to be in contact.

Moreover, it is noted that the bipolar device of Fig. 7-75(a) of the Wolf reference cited by the Examiner appears to be isolated from the FET device by a trench. Thus, it appears that to combine the references in the manner suggested by the Examiner, one of ordinary skill would need to ignore the explicit instructions of the Examiner's citation to the Wolf reference.

Still further, it is noted that in the device of the Examiner's citations to the Manning reference, the emitter region 36 and the source region 36 are the same region 36 as shown in Figs. 7 and 8 of the Manning reference. By contrast, claim 1 requires that "the source region of the first conduction type is formed structurally isolated from the first emitter region of the first conduction type ..."

It is the Examiner's position that the region 40 of the Manning reference is the source region rather than region 36 and that the "source region 40 of the first conduction type [of the Manning reference] is formed structurally isolated from the first emitter region 36 of the first conduction type, by virtue of being separated by a portion of the first body region 26c."

December 16, 2003 Office Action, page 14. Again, it is respectfully submitted that the Examiner is factually mistaken.

Column 6, lines 1-32 cited by the Examiner explicitly states that the region 36 is the *source* region:

> "Yet another alternate embodiment is shown with respect to FIG. 7. ... Here, field oxide region 14g that previously separated collector contact 40 from emitter 36 has been replaced with a FET isolation gate 50. This results in the addition of a parallel NMOS/first conductivity type device between collector 22, C and emitter 36, E (FIG. 8) with its substrate body being tied to bipolar transistor base 26, B. This can provide an additional current drive from **emitter 36 (source)** to collector 22 (drain) at low base biases. Manning reference, col. 5, line 66 – col. 6, line 10. [Emphasis added.]

See also Fig. 8 of the Manning reference which clearly shows the source/emitter "S/E" as one rather than separate.

It is the Examiner's position that the rejection relies upon Fig. 9 of the Manning reference rather than Figs. 7, 8. However, the rejection cites column 6, lines 1-32 (December 16, 2003 Office Action, page 6) which clearly describe Figs. 7 and 8 as well as Fig. 9. Moreover, the Manning reference makes clear that there are only slight differences between the embodiments of Fig. 7 and Fig. 9 which do not affect functionality:

> "FIG. 7 depicts an embodiment wherein base region 26b extends only partially beneath isolation gate 50. FIG. 9 shows an alternate embodiment wherein a base region 26c extends completely beneath isolation gate 50, and joins with collector contact region 40. This should not change the functionality of the bipolar device where spacing between emitter 36 and collector 22 is greater than the base 26c width under middle region 36." Manning reference, col. 6, lines 25-32.

Thus, it is clear that the region 36 depicted in both Fig. 7 and 9 is the source region in both figures. It is further clear that the Examiner has provided no explanation as to why one of ordinary skill would ignore that portion of the Manning reference which describes forming the emitter and the source from the same semiconductor region 36 yet be motivated by the

descriptions of the base and body regions 26c of the Manning reference. The deficiencies of the Examiner's citations to the Wolf and Manning references are not met by the Examiner's citations to the Schwank reference.

Claims 12-14 depend from claim 1 and are allowable for at least the reasons set forth above with respect to claim 1. It is therefore respectfully submitted that the references have been improperly combined and that the rejection of the claims based upon this improper combination should be withdrawn.

The Examiner has made various comments concerning the obviousness of certain features of the present inventions. Applicant respectfully disagrees. Also, the Examiner's comments are deemed moot in view of the above response.

In the statements of reasons for allowance of certain claims the Examiner provided various reasons for allowance. Applicant notes that the claims are directed to various combinations of features. It is respectfully submitted that the patentability of each of the allowed and allowable claims resides in the combination of features recited in that claim in addition to any features noted by the Examiner.

In view of all of the above, it is respectfully submitted that the present application is now in condition for allowance. Reconsideration and reexamination are respectfully requested and allowance at an early date is earnestly solicited.

Respectfully submitted,

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Alan S. Raynes

Alan S. Raynes **February 17, 2004**
Date